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(57) **ABSTRACT**

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FIG. 6

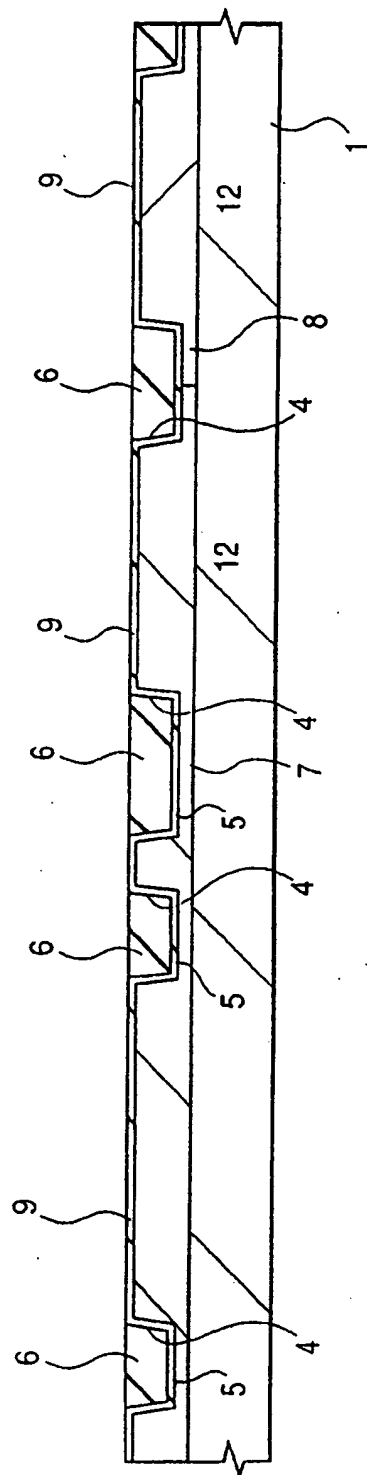
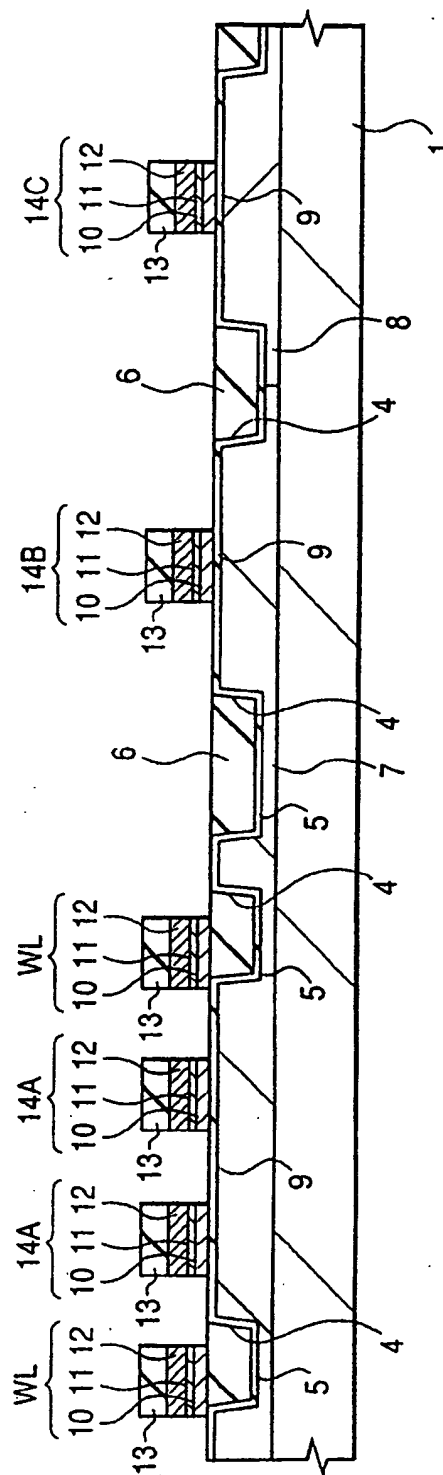


FIG. 7



with a photoresist film as a mask. The silicon oxide film 2 is formed in order to relax a stress to be added to the substrate when another silicon oxide film to be embedded inside of an element isolating groove is densified (sintered) later. The silicon nitride film 3 is resistant to oxidation so that it is used as a mask for preventing the oxidation of the surface of the substrate below the silicon nitride film (active region).

[0155] As illustrated in FIG. 3, the silicon oxide film 2 and semiconductor substrate 1 are dry etched with the silicon nitride film 3 as a mask, whereby a groove 4a (element isolating groove) having a depth of about 300 to 400 nm is formed in an element isolating region of the semiconductor substrate 1.

[0156] As illustrated in FIG. 4, in order to remove a damage layer formed on an inside wall of the groove 4a by the above-described etching, the semiconductor substrate 1 is heat treated to form a silicon oxide film 5 having a film thickness of about 10 nm on the inside wall of the groove 4a. Then, over the semiconductor substrate 1, a silicon oxide film 6 is deposited by the CVD method (embedded from outside with an embedding material. Instead of CVD, SOG or the like method can be employed for the formation of an insulation film). For the improvement of the film quality of the silicon oxide film 6, the semiconductor substrate 1 is heat treated to densify (sinter) the silicon oxide film 6. With the silicon nitride film 3 as a stopper, the silicon oxide film 6 except the inside of the groove 4a is polished by the chemical mechanical polishing (CMP) method, whereby an element isolation groove 4 is formed. (It is needless to say that the term "chemical mechanical polishing" as used herein means not only the polishing by suspended abrasives but also mechanical flattening of the element formation surface.)

[0157] In the next place, the silicon nitride film 3 remaining on the semiconductor substrate 1 is removed by wet etching with hot phosphoric acid. Ions (boron) are then implanted to a region (memory array) in which a memory cell is to be formed and to a region (n-channel type MISFETQn) in which a portion of a peripheral circuit is to be formed, each over the semiconductor substrate 1, whereby a p-type well 7 is formed. On the other hand, P (phosphorus) ions are implanted to a region in which another portion of the peripheral circuit (p-channel type MISFETQp) is to be formed, whereby an n-type well 8 is formed.

[0158] As illustrated in FIG. 6, the silicon oxide film 2 over the surfaces of the p-type well 7 and n-type well 8 is removed using an HF (hydrofluoric acid) type detergent. Then, the semiconductor substrate 1 is wet oxidized, whereby a clean gate oxide film 9 having a thickness of 5 nm or so is formed over the surfaces of the p-type well 7 and n-type well 8.

[0159] Although no particular limitation is imposed, oxidation and nitriding treatment for the segregation of nitrogen at the interface between the gate oxide film 9 and semiconductor substrate 1 may be carried out after the formation of the gate oxide film 9 by thermally treating the semiconductor substrate 1 in an NO (nitrogen oxide) or N<sub>2</sub>O (dinitrogen monoxide) atmosphere. When the gate oxide film 9 becomes as thin as about 5 nm, distortion occurring at the interface due to the difference in a thermal expansion coefficient between the gate oxide film 9 and the semiconductor sub-

strate 1 becomes apparent, which induces the generation of hot carriers. Segregation of nitrogen at the interface with semiconductor substrate 1 relaxes the above distortion so that the above oxidation and nitriding treatment brings about an improvement in the reliability of the ultra-thin gate oxide film 9.

[0160] As illustrated in FIG. 7, a gate electrode 14A (word line WL) and gate electrodes 14B, 14C, each having a gate length of about 0.25  $\mu$ m, are formed over the gate oxide film 9. The gate electrode 14A (word line WL) and gate electrodes 14B, 14C are formed by depositing by CVD, over the semiconductor substrate 1, a polycrystalline silicon film 10 of about 70 nm thick in which n-type impurities such as P (phosphorus) have been doped, depositing thereon a WN film 11 of about 30 nm thick and a W film 12 of about 100 nm thick by sputtering, depositing thereon a silicon nitride film 13 of about 150 nm thick and then patterning these films with a photoresist as a mask.

[0161] When a portion of the gate electrode 14A (word line WL) is formed of a low-resistance metal (W), its sheet resistance can be reduced even to 2  $\Omega/\square$ , which makes it possible to reduce a word line delay. In addition, the delay of word line can be reduced without lining the gate electrode 14 (word line WL) with an AL interconnection or the like so that the number of the interconnection layers to be formed over the memory cell can be reduced by one.

[0162] Then, the photoresist is removed by ashing treatment, followed by removal of the dry etching residue or ashing residue on the semiconductor substrate 1 by an etching liquid such as hydrofluoric acid. By this wet etching, as illustrated in FIG. 8, the gate oxide film 9 of the regions other than those below the gate electrode 14A (word line WL) and not-illustrated gate electrodes 14B, 14C and also the gate oxide film 9 at the lower portions of the side walls of the gate are isotropically etched and undercuts appear, leading to an inconvenience such as lowering in the pressure resistance of the gate oxide film 9. Here, re-oxidation (light oxidation) treatment is carried out by the below-described process in order to regenerate the impaired gate oxide film 9.

[0163] FIG. 9(a) is a schematic plan view illustrating one example of a specific constitution of a single-wafer-process type oxidizing furnace to be used for the light oxidation treatment and FIG. 9(b) is a cross-sectional view taken along a line B-B' of FIG. 9(a).

[0164] The single-wafer-process type oxidizing furnace 100 is equipped with a chamber 101 made of a multiple-wall quartz tube, and above and below the chamber, heaters 102a and 102b are disposed for heating a semiconductor wafer 1A, respectively. Inside the chamber 101, housed is a disk-shaped soaking ring 103 for uniformly dispersing the heat supplied from the heaters 102a, 102b all over the semiconductor wafer 1A and above the ring, a susceptor 104 for horizontally holding the semiconductor wafer 1A is disposed. The soaking ring 103 is made of a heat-resistant material such as quartz or SiC (silicon carbide), and is supported by a supporting arm 105 which extends from the wall surface of the chamber 101. In the vicinity of the soaking ring 103 installed is a thermocouple 106 for measuring the temperature of the semiconductor wafer 1A supported by the susceptor 104. For heating of the semiconductor wafer 1A, heating system by a lamp 107 as



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438/592  
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	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 20010033027 A1	20011025	9	Graded layer for use in semiconductor circuits and	257/763	257/412; 257/768;
2	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 20010020707 A1	20010913	15	Semiconductor device and method for fabricating the	257/288	257/408; 257/412;
3	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 20010019868 A1	20010906	18	Field effect transistor assemblies, integrated	438/275	438/592
4	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 20010018243 A1	20010830	12	Method for fabricating a semiconductor device	438/221	438/231; 438/592
5	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 20010005622 A1	20010628	5	Method for manufacturing gate electrode with vertical	438/592	438/720
6	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 20010002071 A1	20010531	9	Boron incorporated diffusion barrier material	257/751	257/412; 438/592;
7	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 20010000629 A1	20010503	11	Semiconductor device and process of producing the	257/388	438/585; 438/592
8	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6344380 B1	20020205	7	Manufacturing of gate electrodes having silicon of	438/197	438/198; 438/199;
9	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6340629 B1	20020122	6	Method for forming gate electrodes of semiconductor	438/592	438/652; 438/653;
10	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6333250 B1	20011225	6	Method of forming gate electrode in semiconductor	438/595	438/592
11	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6326260 B1	20011204	8	Gate prestackers for high density, high performance	438/241	438/592; 438/595;

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14	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6284635 B1	20010904	7	Method for forming titanium polycide gate	438/592	438/652; 438/656;
15	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6277736 B1	20010821	5	Method for forming gate	438/653	438/303; 438/592;
16	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6277722 B1	20010821	5	Method for forming poly metal gate	438/592	438/299; 438/303;
17	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6277699 B1	20010821	6	Method for forming a metal-oxide-semiconductor	438/303	438/305; 438/592;
18	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6194294 B1	20010227	5	Method of forming gate electrode in semiconductor	438/585	438/592; 438/593;
19	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6165863 A	20001226	9	Method for forming multilayer sidewalls on a	438/592	257/900; 438/265;
20	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6130145 A	20001010	7	Insitu doped metal polycide	438/592	438/655
21	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6080645 A	20000627	7	Method of making a doped silicon diffusion barrier	438/585	438/588; 438/591;
22	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5888588 A	19990330	8	Process for forming a semiconductor device	427/248.1	427/255.392; 427/255.7;
23	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5877074 A	19990302	6	Method for improving the electrical property of gate	438/592	
24	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5767004 A	19980616	9	Method for forming a low impurity diffusion	438/592	438/197; 438/301

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4	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 20010018243 A1	20010830	12	Method for fabricating a semiconductor device	438/221	438/231; 438/592
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6	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 20010002071 A1	20010531	9	Boron incorporated diffusion barrier material	257/751	257/412; 438/592;
7	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 20010000629 A1	20010503	11	Semiconductor device and process of producing the	257/388	438/585; 438/592
8	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6344380 B1	20020205	7	Manufacturing of gate electrodes having silicon of	438/197	438/198; 438/199;
9	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6340629 B1	20020122	6	Method for forming gate electrodes of semiconductor	438/592	438/652; 438/653;
10	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6333250 B1	20011225	6	Method of forming gate electrode in semiconductor	438/595	438/592
11	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6326260 B1	20011204	8	Gate prestackers for high density, high performance	438/241	438/592; 438/595;
12	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6306743 B1	20011023	9	Method for forming a gate electrode on a semiconductor	438/592	257/413; 438/653
13	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6297137 B1	20011002	5	Method for forming gate electrode in semiconductor	438/592	438/682

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1	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 20010019868 A1	20010906	18	Field effect transistor assemblies, integrated	438/275	438/592	4
2	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 20010005622 A1	20010628	5	Method for manufacturing gate electrode with vertical	438/592	438/720	4
3	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 20010002071 A1	20010531	9	Boron incorporated diffusion barrier material	257/751	257/412; 438/592;	4
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5	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6306743 B1	20011023	9	Method for forming a gate electrode on a semiconductor	438/592	257/413; 438/653	4
6	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6194294 B1	20010227	5	Method of forming gate electrode in semiconductor	438/585	438/592; 438/593;	4
7	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6165883 A	20001226	9	Method for forming multilayer sidewalls on a	438/592	257/900; 438/265;	4
8	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6080645 A	20000627	7	Method of making a doped silicon diffusion barrier	438/585	438/588; 438/591;	4
9	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5888588 A	19990330	8	Process for forming a semiconductor device	427/248.1	427/255.392; 427/255.7;	4
10	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5877074 A	19990302	6	Method for improving the electrical property of gate	438/592		4